IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application Serial No. 08/530,661
Filing Date . . . . . September 20, 1995
Inventor . . . . . Brent Keeth et al.
Assignee . . . . . Micron Technology, Inc.
Group Art Unit 2503
Examiner . . . . . N. Kelly
Attorney's Docket No. MI22-356
Title: Semiconductor Memory Circuitry

BRIEF OF APPELLANT

To: Assistant Commissioner For Patents
Washington, D.C. 20231

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Appellant appeals from the final rejection, mailed September 23, 1997, of Claims 6-10, 18-19, 22-23 and 25-26. This brief is submitted in triplicate. A check for $1,260 is attached, including the amount of $310.00 in payment of the filing fee required under 37 C.F.R. §1.17(f) and also including the amount of $950 for the three-month extension fee due under 37 C.F.R. §1.17(c).

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I. REAL PARTY IN INTEREST.

The real party in interest of this application is Micron Technology, Inc. as evidenced by the full assignment of the pending application to Micron Technology, Inc. recorded at Reel 7671, Frame 0965 in the Assignment Branch of the Patent and Trademark Office.

II. RELATED APPEALS AND INTERFERENCES.

Appellant, Appellant's undersigned legal representative, and the assignee of the pending application are aware of no appeals or interferences which will directly affect, be directly affected by, or have a bearing on the Board's decision in the pending appeal.

III. STATUS OF THE CLAIMS.

Claims 6-10, 18-19, 22-23 and 25-26 are pending, stand finally rejected, and are being appealed.

IV. STATUS OF AMENDMENTS.

No amendment to the application has been submitted subsequent to final rejection.

V. SUMMARY OF THE INVENTION.

The claimed inventions are memory die or devices having smaller size or consumed monolithic die area than did prior art devices. (*See*, specification at pg. 34, lns. 20-23.) In one aspect, the claimed invention

encompasses a 16M semiconductor memory device comprising a total of from 16,000,000 to 17,000,000 functional and operably addressable memory cells occupying an area on a semiconductor die which is no greater than 14 mm^2. (*See, for example*, specification at pg. 37, lns. 15-21.)

In another aspect, the above-mentioned 16M semiconductor memory device further comprises peripheral circuitry and pitch circuitry formed on the die relative to the memory arrays. (*See, for example*, specification at pg. 37, ln. 24 through pg. 38, ln. 3.) The peripheral circuitry, pitch circuitry and memory arrays have a total combined continuous surface area which is less than or equal to 35 mm^2. (*See, for example*, specification at pg. 38, ln. 3.)

In another aspect, the above-mentioned peripheral circuitry, pitch circuitry and memory arrays have a total combined continuous area on a die which is less than or equal to 32 mm^2. (*See, for example*, specification at pg. 38, lns. 11-14.)

In yet another aspect, the invention encompasses a 16M semiconductor memory device having a total of from 16,000,000 to 17,000,000 functional and operably addressable memory cells arranged in multiple memory arrays. (*See, for example*, specification at pg. 37, lns. 15-18.) At least one of the memory arrays contains at least one area of 100 square microns of continuous die surface area which has at least 128 of the functional and operably addressable memory cells. (*See, for example*, specification at pg. 38, lns. 3-6.)

In another aspect, the above-mentioned at least one area of 100 square microns has at least 170 of the functional and operably addressable memory cells. (*See, for example*, specification at pg. 38, lns. 14-16.)

VI. ISSUE.

Are the inventions of claims 6-10, 18-19, 22-23 and 25-26 sufficiently described in the specification such that a person of ordinary skill in the art is enabled to make and use the inventions within the meaning of 35 U.S.C. § 112 ¶ 1?

VII. GROUPING OF CLAIMS.

Claims 6-10, 18-19, 22-23 and 25-26 stand or fall as one group.

VIII. ARGUMENT.

A. Summary Of The Examiner's Rejections.

Claims 6-10, 18-29, 22-23 and 25-26 stand rejected under 35 U.S.C. § 112 ¶ 1. (Paper 12, pg. 2, ¶ 2.) The Examiner indicates that Applicant's disclosure describes various improvements for producing Applicant's claimed structures, and contends that one or more of such improvements are critical or essential to the practice of Applicant's invention. (Paper 12, pg. 2, ¶ 2.) The Examiner states that since the improvements are not included in Applicant's claims, the claimed structures are not enabled by Applicant's disclosure. (Paper 12, pg. 2,

¶ 2.) *In re Mayhew*, (527 F.2d 1229, 188 USPQ 356 (CCPA 1976)) is cited to support the position that Applicant's claims are not enabled.

The Examiner further states that the need to utilize one or more of Applicant's disclosed improvements to practice Applicant's claimed methods is evidenced by the novelty and non-obviousness of Applicant's invention. (Paper 12, pg. 3, ¶ 3.) Specifically, the Examiner contends that since Applicant's claimed structures were not known in the prior art, Applicant's disclosed methods of forming the structures must be essential for producing such claimed structures. (Paper 12, pg. 3, ¶ 3.)

B. The Specification And Claims Comply With 35 U.S.C. § 112 ¶ 1.

The Examiner is mistaken in his contention that Applicant's claims lack enablement. The *Mayhew* ruling is not applicable to the present case for at least the reason that its facts are not analogous to the present facts.

In *Mayhew*, the court found that an Appellant's specification indicated that certain components were essential for a claimed method invention. (*See*, 188 USPQ at p. 358.) Such essential components pertained to the utilization and location of a cooling apparatus. The *Mayhew* specification stated that a strip and bath are "raised in temperature above what is ordinarily considered optimum coating temperatures. *This is practical because of special cooling apparatus, specially located.*'" (Emphasis by the court) (188 USPQ at p. 358.) Also,

the *Mayhew* specification stated "if high temperature galvanizing spelter were present in zone 54, iron dissolution and dross formation would make it *impossible to produce the smooth coat produced by the present invention.*" (Emphasis added by the court.) (188 USPQ at p. 361.) The *Mayhew* Court determined that the statements of the specification indicated that the cooling apparatus and its location were essential to Mayhew's invention. (*See*, 188 USPQ at p. 358.) As evidenced by the above-quoted sections of Mayhew's specification, it unambiguously stated that the recited invention required (i.e., was impossible without) specific embodiments set forth in the specification. Accordingly, the Court held that method claims failing to recite such essential steps were not enabled by the specification. (*See*, 188 USPQ at p. 358.)

In contrast to the specification of *Mayhew*, Applicant's specification contains no language indicating that Applicant's claims are to be confined solely to disclosed embodiments. To the contrary, Applicant's disclosure states exactly the opposite, that "[o]ne or more of the [disclosed] techniques, or other techniques, can be utilized in the production of 64M, 16M or 4M memory chips in accordance with the invention, with the invention only being limited by the accompanying claims appropriately interpreted in accordance with the Doctrine of Equivalents." (P. 9. lns. 3-7 of Applicant's specification, emphasis added.) The disclosure further states that the specifically disclosed methods of achieving high device density are provided by way of

example only and not by way of limitation. (*See*, for example, p. 37, lns. 21-24; and p. 39, lns. 5-8.)

As the above-discussed statements illustrate, Applicant's disclosure does not expressly limit the invention to the disclosed embodiments, but rather specifically indicates that such limitation is not to occur. Thus, unlike the disclosure at issue in *Mayhew*, Applicant's disclosure cannot reasonably be interpreted to require that any of Applicant's disclosed embodiments are essential to Applicant's claimed inventive structure. For at least this reason, the Examiner's rejections of claims 6-10, 18-19, 22-23 and 25-26 are improper and should be reversed.

The facts of the present case are analogous to those presented in *Beale v. Schuman*, 212 USPQ 291 (BOPI 1980). In *Beale*, the Board explained that *Mayhew* is inapplicable to cases in which an Applicant's disclosure provides nothing requiring claims to be confined solely to disclosed embodiments. (212 USPQ at 293.) The disclosure in *Beale* concerned a free-piston engine with means provided to permit a working gas to leak by the piston. The *Beale* specification only disclosed embodiments in which gas passages were provided on cylinder walls. (*See*, 212 USPQ at pgs. 291, 293.) Yet, a claim in *Beale* was broad enough to encompass structures with gas passages formed on either a cylinder, or on both a piston and a cylinder. (*See*, 212 USPQ at p. 293.) The Board held that the specification was sufficient to enable the scope of the claim, and stated

> We find nothing in the ... disclosure which requires the gas passages to be confined solely to the cylinder walls. . . An inventor is not required to limit his claims to a specific example or examples disclosed in his application.

(212 USPQ at p. 293.) From the Board's discussion in *Beale*, it is apparent that *Mayhew* should be invoked to narrow claims only when a disclosure indicates that particular steps are required for a claimed invention. A mere description of specific enabling embodiments or examples is not enough to indicate that particular steps are required for an invention. Rather, express language indicating such requirement must be in a disclosure before *Mayhew* is applicable. Such express language was provided in *Mayhew*'s disclosure with the statement that certain results were, a) only "practical" due to specific embodiments set forth by *Mayhew*; and b) essentially "impossible" without the embodiment which produced acceptable inventive results.

Applicant's disclosure, like the disclosure at issue in *Beale*, contains no language indicating that Applicant's claims are to be confined solely to disclosed embodiments. It does just the opposite. Thus, for the reasons discussed in *Beale*, Applicant's claims should not be limited to Applicant's disclosed embodiments. The Examiner's rejections of claims 6-10, 18-19, 22-23 and 25-26 are therefore improper and should be reversed.

Further, the claims in *Mayhew* were method, wherein the claims in *Beale* were article. Applicant's appealed claims are also article. Accordingly, the instant facts are analogous to *Beale*, not *Mayhew*, and

the *Beale* ruling should be applied here. With respect to *article* claims, the Board in *Beale* held,

> "broad claims may be supported by a specific embodiment ... and an inventor need not limit his claims to precisely what he has found will work..." (*Beale* at p. 294.)

Likewise, Applicant has submitted article claims and should not be compelled to limit such claims to certain disclosed *methods* by which such are producible. To require such would be to essentially compel product-by-process claims, which is not what Applicant "regards" as its invention in the presentation of the appealed claims. Applicant should not be limited to such claims, even under *Mayhew*, as there is no indicated requirement or necessity of any method limitations presented by the specification. Regardless, *Beale* is controlling with respect to Applicant's article claims, not *Mayhew*. Applicant's claims are inherently in compliance with 35 U.S.C. §112, and under the authority of *Beale*.

A final thrust of the Examiner's rejection is an attempt to utilize the novelty and non-obviousness of Applicant's claimed structure as evidence that Applicant's disclosed embodiments are essential to the claimed invention. Such is clearly an improper basis for rejection. Applicant is aware of no authority indicating that the novelty and non-obviousness of an invention has any bearing on whether an invention is enabled, and contends that there is none. If the Examiner's basis of rejection were accurate, then every claim to novel and non-obvious structures would need to be limited to only the embodiments specifically disclosed in the specification accompanying the claim. Clearly, the

Examiner's basis of rejection cannot be accurate. For instance, every issued patent claim is presumed to be novel and non-obvious, (35 U.S.C. §282), yet every issued claim is not limited to only the embodiments specifically disclosed in the specification accompanying the claim. (*See, e.g., Beale.*) Accordingly, the novelty and non-obviousness of an invention is irrelevant to whether the invention is enabled. For this additional reason the Examiner's rejections of claims 6-10, 18-19, 22-23 and 25-26 under 35 U.S.C. § 112 ¶ 1 are improper and should be reversed.

C. Conclusion.

For the above-discussed reasons, the Examiner's rejections of claims 6-10, 18-19, 22-23 and 25-26 are improper. Applicant therefore requests reversal of the final rejections of claims 6-10, 18-19, 22-23 and 25-26. Allowance of such claims is also respectfully requested.

Respectfully submitted,

Dated: 3/23/05 By: _____

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IX. APPENDIX A -- THE CLAIMS INVOLVED IN THIS APPEAL.

6. A 16M semiconductor memory device comprising:

a semiconductor die encapsulated in a package, the package having an encapsulating body and electrically conductive interconnect pins extending outwardly from the body;

a total of from 16,000,000 to 17,000,000 functional and operably addressable memory cells arranged in multiple memory arrays formed on the die, the individual functional and operably addressable memory cells occupying area on the die within the memory arrays, the occupied area of all functional and addressable memory cells on the die having a total combined area which is no greater than 14 mm^2; and

peripheral circuitry and pitch circuitry formed on the die relative to the memory arrays; the peripheral circuitry electrically interconnecting with the pins and including operably interconnected control and timing circuitry, address and redundancy circuitry, data and test path circuitry, and voltage supply circuitry which collectively enable full access to all addressable memory cells of the memory arrays.

7. The semiconductor memory device of claim 6 wherein the peripheral circuitry, the pitch circuitry, and the memory arrays are fabricated to include a total of four or less conductive line layers.

8. The semiconductor memory device of claim 6 wherein the peripheral circuitry, the pitch circuitry and the memory arrays have a total combined continuous surface area on the die which is less than or equal to 35 mm^2.

9. The semiconductor memory device of claim 6 wherein the peripheral circuitry, the pitch circuitry, and the memory arrays are fabricated to include at least five conductive line layers, the occupied area of all functional and operable memory cells on the die having a total combined area on the die which is no greater than 11 mm^2.

10. The semiconductor memory device of claim 6 wherein the peripheral circuitry, the pitch circuitry, and the memory arrays are fabricated to include at least five conductive line layers; the peripheral circuitry, the pitch circuitry and the memory arrays having a total combined continuous surface area on the die which is less than or equal to 32 mm^2.

18. A 16M semiconductor memory device comprising:

a semiconductor die encapsulated in a package, the package having an encapsulating body and electrically conductive interconnect pins extending outwardly from the body;

a total of from 16,000,000 to 17,000,000 functional and operably addressable memory cells arranged in multiple memory arrays formed on the die, at least one of the memory arrays containing at least one area of 100 square microns of continuous die surface area having at least 128 of the functional and operably addressable memory cells; and

peripheral circuitry and pitch circuitry formed on the die relative to the memory arrays; the peripheral circuitry electrically interconnecting with the pins and including operably interconnected control and timing circuitry, address and redundancy circuitry, data and test path circuitry, and voltage supply circuitry which collectively enable full access to all addressable memory cells of the memory arrays.

19. The semiconductor memory device of claim 18 wherein at least one of the memory arrays containing at least one area of 100 square microns of continuous die surface area has at least 170 of the functional and operably addressable memory cells.

22. A semiconductor memory device comprising:

a total of no more than 68,000,000 functional and operably addressable memory cells arranged in multiple memory arrays formed on a semiconductor die; and

circuitry formed on the semiconductor die permitting data to be written to and read from one or more of the memory cells, at least one of the memory arrays containing at least one area of 100 square microns of continuous die surface area having at least 128 of the functional and operably addressable memory cells.

23. The semiconductor memory device of claim 22 wherein the total number of functional and operably addressable memory cells on the semiconductor die is no more than 17,000,000.

25. The semiconductor memory device of claim 22 wherein at least one of the memory arrays containing at least one area of 100 square microns of continuous die surface area has at least 170 of the functional and operably addressable memory cells.

26. The semiconductor memory device of claim 22 wherein at least one of the memory arrays containing at least one area of 100 square microns of continuous die surface area has at least 170 of the functional and operably addressable memory cells, and the total number of functional and operably addressable memory cells on the semiconductor die is no more than 17,000,000.